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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,673	02/25/2002	Michio Nemoto	FUJI:212	9446
7590	12/18/2003		EXAMINER	
ROSSI & ASSOCIATES				ANDUJAR, LEONARDO
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				ART UNIT
				PAPER NUMBER
				2826

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,673	NEMOTO ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 26 September 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 3,8-16 and 18-33 is/are pending in the application.
4a) Of the above claim(s) 3,8,14-16 and 18-23 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 9-13 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 02/25/2002 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) The translation of the foreign language provisional application has been received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 09/28/02
4) Interview Summary (PTO-413) Paper No(s)
5) Notice of Informal Patent Application (PTO-152)
6) Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, Species 1 (claims 9-13) in a communication filed on 09/26/2003 is acknowledged.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. Figure 25 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (JP-2000223720, cited by Applicant).

7. Regarding claims 9 and 10, Yamada (see fig. 5 & machine translation) shows most aspects of the instant invention including a semiconductor device comprising a drift layer (1, 9) of a first conductivity type having a first major surface and a second major surface; an anode layer 2 of a second conductivity type on the first major surface of the drift layer, the anode layer being doped more heavily than the drift layer; a cathode layer 3 of the first conductivity type on the second major surface of the drift layer, the cathode layer being doped more heavily than the drift layer; and a buffer layer 6 of the first conductivity type extending across the drift layer, the buffer layer being spaced apart from the anode layer and the cathode layer, the buffer layer being doped more heavily than the drift layer. Yamada teaches that the drift layer includes a sublayer 1. The thickness of sublayer 1 "W_i" is equal to a distance "X₁" from the pn junction between the anode layer and the drift layer to the edge of the buffer layer on the side of the anode. Yamada discloses that this thickness or the distance "X₁" is a variable subject to optimization (abstract). Yamada does not explicitly disclose that the distance X₁ can be expressed by one of the following relational expressions:

$$0.3 \leq X_1 / \{ (BV \epsilon_s) / q [(J_F / q v_{sat}) + N_D] \}^{1/2} \leq 1.6$$

$$0.8 \leq X_1 / \{ (BV \epsilon_s) / q [(J_F / q v_{sat}) + N_D] \}^{1/2} \leq 1.2$$

where BV is the breakdown voltage of the semiconductor device, ϵ_s is the dielectric permitivity of the semiconductor, q is the elementary charge quantity, J_F is the rated current density of the semiconductor device, v_{sat} is the carrier saturation velocity, and N_D is the concentration of the impurity of the first conductivity type in the drift layer. Nonetheless, the specific thickness range claimed by applicant, is only considered to be the "optimum" thickness range for the drift sublayer disclosed by the Yamada that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see *In re Boesch*, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as the drift sublayer is used as already suggested by the Yamada.

8. Regarding claim 11, Yamada (e.g. fig. 5) shows most aspects of the instant invention including a semiconductor device comprising a drift layer (1, 9) of a first conductivity type having a first major surface and a second major surface; an anode layer 2 of a second conductivity type on the first major surface of the drift layer, the anode layer being doped more heavily than the drift layer; a cathode layer 3 of the first conductivity type on the second major surface of the drift layer, the cathode layer being doped more heavily than the drift layer; and a buffer layer 6 of the first conductivity type

extending across the drift layer, the buffer layer being spaced apart from the anode layer and the cathode layer, the buffer layer being doped more heavily than the drift layer. Yamada discloses that the thickness and the average impurity concentration of the buffer layer N_{D2} are variables subjected to optimization (PP12-23). Yamada does not explicitly disclose that the thickness of the buffer layer Y_1 and the average impurity concentration of the buffer layer N_{D2} can be expressed by the following relational expressions:

$$Y_1 / \{ [X_1^2 + 2\epsilon_s(V_{CC} + V_{PT})/q N_{D2}]^{1/2} - X_1 \} \leq 2$$

where X_1 is the shortest distance from the pn-junction between the anode layer and the drift layer to the edge of the buffer layer on the side of the anode, V_{CC} is the half value of the breakdown voltage of the semiconductor device, V_{PT} is the voltage, at which the depletion layer contacts the buffer layer of the first conductivity type, ϵ_s is the dielectric permittivity of the semiconductor, and q is the elementary charge quantity. Nonetheless, the specific thickness and concentration claimed by applicant, are only considered to be the "optimum" thickness and impurity concentration of the buffer layer disclosed by the Yamada that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see *In re Boesch*, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as the buffer layer is used as already suggested by the Yamada.

9. Regarding claims 12 and 3, Yamada discloses most aspects of the instant invention including a buffer layer having an average impurity concentration (see comments above). Yamada discloses that the thickness and the average impurity concentration of the buffer layer N_{D2} are variables subjected to optimization (PP12-23). Yamada does not explicitly disclose that the thickness of the buffer layer Y_1 and the average impurity concentration of the of the buffer layer N_{D2} can be expressed by the following relational expressions:

$$Y_1 / \{ [X_1^2 + 2\epsilon_s(V_{CC} + V_{PT})/q N_{D2}]^{1/2} - |X_1| \} \leq 2$$

where X_1 is the shortest distance from the pn-junction between the anode layer and the drift layer to the edge of the buffer layer on the side of the anode, V_{CC} is the half value of the breakdown voltage of the semiconductor device, V_{PT} is the voltage, at which the depletion layer contacts the buffer layer of the first conductivity type, ϵ_s is the dielectric permittivity of the semiconductor, and q is the elementary charge quantity. Nonetheless, the specific thickness and concentration claimed by applicant, are only considered to be the "optimum" thickness and impurity concentration of the buffer layer disclosed by the Yamada that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see *In re Boesch*, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as the buffer layer is used as already suggested by the Yamada.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kitagawa and Fuji disclose structures and procedures similar to the instant invention.

11. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722 or -7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2814 applications.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

13. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900**.

Leonardo Andújar
Patent Examiner Art Unit 2826
LA
12/9/03

NATHAN J. FLYNN
PERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800